IN THE TITLE:

The title has been amended herein. Pursuant to 37 C.F.R. §§ 1.121 and 1.125 (as amended to date), please enter the title as amended.

~~FLIP CHIP~~FLIP-CHIP TECHNIQUE FOR CHIP ASSEMBLY

IN THE SPECIFICATION:

Please replace paragraph number **[0003]** with the following rewritten paragraph:

[0003] State of the Art: A ~~flip chip~~ flip-chip is a semiconductor chip or die that has bumped terminations spaced around the active surface of the die and is intended for face-to-face attachment to a substrate or another semiconductor die. The bumped terminations of the ~~flip chips~~ flip-chips are usually a "Ball Grid Array" ("BGA") configuration wherein an array of minute solder balls is disposed on an attachment surface of a semiconductor die, or a "Slightly Larger than Integrated Circuit Carrier" ("SLICC") configuration wherein an array of minute solder balls is disposed on an attachment surface of a semiconductor die similar to a BGA, but having a smaller solder ball pitch and diameter than a BGA.

Please replace paragraph number **[0004]** with the following rewritten paragraph:

[0004] The attachment of a ~~flip chip~~ flip-chip to a substrate or another semiconductor involves aligning the solder balls on the ~~flip chip~~ flip-chip with a plurality of contact points (configured to be a mirror image of the solder ball arrangement on the ~~flip chip~~ flip-chip) on a facing surface of the substrate. A plurality of solder balls may also be formed on a facing surface of the substrate at the contact points. A quantity of liquid flux is often applied to the face of the chip and/or substrate, and the chip and substrate are subjected to elevated temperature to effect refluxing or soldering of the solder balls on the chip and/or corresponding solder balls on the substrate.

Please replace paragraph number **[0005]** with the following rewritten paragraph:

[0005] There are numerous variations to the standard ~~flip chip~~ flip-chip attachment technique. For example, U.S. Patent 5,329,423 issued July 12, 1994 to Scholz relates to a demountable ~~flip chip~~ flip-chip assembly comprising a first substrate having a contact site with a raised bump and a second substrate having a depression for a contact site. The raised bumps are pressed into the depressed areas to electrically and mechanically connect the first substrate to the

second substrate without using reflowed solder. Thus, the first substrate can be removed from the second substrate without damaging either substrate.

Please replace paragraph number **[0006]** with the following rewritten paragraph:

[0006] U.S. Patent 5,477,086 issued December 19, 1995 to Rostoker et al. relates to a ~~flip-chip~~ flip-chip attachment technique involving forming a concave conductive bump on one substrate (such as the PCB) to receive and align the solder balls on the other substrate (such as the semiconductor die). The solder balls and/or the concave conductive bump are reflowed to fuse them together.

Please replace paragraph number **[0008]** with the following rewritten paragraph:

[0008] Such ~~flip-chip~~ flip-chip and substrate attachments (collectively "electronic packages") are generally comprised of dissimilar materials that expand at different rates on heating. The most severe stress is due to the inherently large thermal coefficient of expansion ("TCE") mismatch between the plastic and the metal. These electronic packages are subject to two types of heat exposures: process cycles, which are often high in temperature but few in number; and operation cycles, which are numerous but less extreme. If either the ~~flip-chip~~ flip-chip(s) and/or substrate(s) are unable to repeatedly bear their share of the system thermal mismatch over its lifetime, the electronic package will fracture, thereby destroying the functionality of the electronic package.

Please replace paragraph number **[0016]** with the following rewritten paragraph:

[0016] The second substrate is preferably a ~~flip-chip~~ flip-chip, such as a memory chip, a CPU, or a logic chip. ~~Flip-chips~~ Flip-chips are generally manufactured with a plurality of bond pads on an active surface wherein each bond pad is connected to a lead. A facing surface of each bond pad has the conductive bump formed thereon.

Please replace paragraph number **[0031]** with the following rewritten paragraph:

[0031] FIG. 2 illustrates a second substrate or flip-chip component 200 of the present invention. The flip-chip component 200 comprises a second substrate or semiconductor die 202 having a plurality of bond pads 204 on a facing surface 206 of the semiconductor die 202. Each bond pad 204 is connected to a trace lead 208 (shown by a dashed line) on a lower bond pad surface 210. A facing surface 212 of each bond pad 204 has a conductive pad 214 formed thereon. A passivation layer 216 is applied over the semiconductor die facing surface 206. The passivation layer 216 is etched by any known industry standard technique to form vias 218 to expose a facing surface 220 of the semiconductor die conductive pad 214. It is, of course, understood that, rather than etching the passivation layer 216, a masking technique could be employed, such as a silk screen, over the semiconductor die conductive pad facing surface 220 when applying the passivation ~~layer 214~~ layer 216.

Please replace paragraph number **[0032]** with the following rewritten paragraph:

[0032] FIG. 3 illustrates a first substrate/second substrate assembly 300 of the present invention. The first substrate/second substrate assembly 300 is a combination of the first substrate component 100 of FIG. 1 and the second substrate or flip-chip component 200 of FIG. 2; therefore, components common to FIGS. 1, 2, and 3 retain the same numeric designation. The substrate conductive pads 108 and the semiconductor die conductive pads 214 are aligned to be the mirror-image of one another, such that when the flip-chip component 200 is flipped to attach to the first substrate component 100, each substrate conductive pad 108 contacts its respective semiconductor die conductive pad 214. Thus, the substrate/flip-chip assembly 300 is constructed by flipping the flip-chip component 200 and attaching the flip-chip component 200 to the first substrate component 100. A layer of adhesive 302 is disposed between the passivation layer 216 and the first substrate facing surface 106. When the flip-chip component 200 is attached to the first substrate component 100, a facing surface 304 of the first substrate conductive pad 108 and the semiconductor die conductive pad facing surface 220 come into electrical communication without being attached to one another. It is, of course, understood

that the passivation layer could be applied to the first substrate active surface, etched, and adhered to the second substrate active surface.

Please replace paragraph number **[0033]** with the following rewritten paragraph:

[0033] FIG. 4 illustrates a first alternative first substrate/second substrate assembly 400 of the present invention. The first ~~alternate~~ alternative first substrate/second substrate assembly 400 is similar to the first substrate/second substrate assembly 300 of FIG. 3; therefore, components common to FIGS. 3 and 4 retain the same numeric designation. The first alternative first substrate/second substrate assembly 400 differs from the first substrate/second substrate assembly 300 in that the second substrate or flip-chip component 200 is specifically a substrate with the conductive pad 214 formed on a substrate lead 402, rather than on a ~~flip chip~~ flip-chip type bond pad 204 connected to a trace lead 208 shown in FIG. 3. The first alternative first substrate/second substrate assembly 400 also differs from the first substrate/second substrate assembly 300 in that the passivation layer 216 is first applied to first substrate facing surface 106, then a layer of adhesive 802 is disposed between the passivation layer 216 and the second substrate 202.

Please replace paragraph number **[0034]** with the following rewritten paragraph:

[0034] FIG. 5 illustrates a second alternative first substrate/second substrate assembly 500 of the present invention. The second ~~alternate~~ alternative first substrate/second substrate assembly 500 is similar to the first substrate/second substrate assembly 300 of FIG. 3; therefore, components common to FIG. 3 and FIG. 5 retain the same numeric designation. The second alternative first substrate/second substrate assembly 500 differs from the first substrate/second substrate assembly 300 in that a glob top material 502 is used to attach the second substrate or flip-chip component 200 to the first substrate component 100, rather than using the layer of adhesive 302 shown in FIG. 3.

Please replace paragraph number **[0035]** with the following rewritten paragraph:

[0035] FIG. 6 illustrates a third alternative first substrate/second substrate assembly 600 of the present invention. The third ~~alternate~~ alternative first substrate/second substrate assembly 600 is similar to the first substrate/second substrate assembly 300 of FIG. 3; therefore, components common to FIGS. 3 and 6 retain the same numeric designation. The third alternative first substrate/second substrate assembly 600 differs from the first substrate/second substrate assembly 300 in that an encapsulant material 602 is used to substantially encase and attach the second substrate or flip-chip component 200 together with the first substrate component 100, rather than using the layer of adhesive 302 shown in FIG. 3.

Please replace paragraph number **[0036]** with the following rewritten paragraph:

[0036] FIG. 7 illustrates a fourth alternative first substrate/second substrate assembly 700 of the present invention. The fourth ~~alternate~~ alternative first substrate/second substrate assembly 700 is similar to the first substrate/second substrate assembly 300 of FIG. 3; therefore, components common to FIGS. 3 and 7 retain the same numeric designation. The fourth alternative first substrate/second substrate assembly 700 differs from the first substrate/second substrate assembly 300 in that a first plurality of grooves 702 is disposed on the facing surface 106 of the first substrate 102 and a second plurality of grooves 704 is disposed on the facing surface 206 of the second substrate 202 wherein the first plurality of grooves 702 intermesh with the second plurality of grooves 704 to assist in preventing or minimizing the movement of first substrate 102 and/or second substrate 202 due to thermal expansion or other mechanical causes.

IN THE CLAIMS:

Claims 5 and 32 were previously cancelled. Claims 2-4, 7 and 9-31 have been amended herein. All of the pending claims are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

1. (Previously presented) An assembly method for a semiconductor assembly, comprising:

providing a first substrate having a facing surface and having at least one lead having a portion thereof located on said facing surface of said first substrate, said at least one lead having at least one conductive pad disposed on the portion thereof located on said facing surface of said first substrate, said at least one conductive pad of said at least one lead of said first substrate having a thickness and having a contact surface area;

providing a second substrate having a facing surface and having at least one lead having a portion thereof located on said facing surface of said second substrate, said at least one lead having at least one conductive pad disposed on the portion thereof located on said facing surface of said second substrate, said at least one conductive pad of said at least one lead of said second substrate having a thickness and having a contact surface area;

providing a passivation layer on said facing surface of said first substrate, said passivation layer having a thickness greater than said thickness of said at least one conductive pad of said at least one lead of said first substrate such that said at least one conductive pad of said at least one lead of said first substrate is recessed a distance within said passivation layer;

forming an opening in said passivation layer at the location of said at least one conductive pad of said at least one lead of said first substrate;

attaching said first substrate to said second substrate, said at least one conductive pad of said at least one lead of said second substrate extending a distance within said opening in said passivation layer of said first substrate;

abutting said contact surface area of said at least one conductive pad of said at least one lead of said first substrate against said contact surface area of said at least one conductive pad of said at least one lead of said second substrate;

forming direct sliding movable contact between said contact surface area of said at least one conductive pad of said at least one lead of said first substrate and said contact surface area of said at least one conductive pad of said at least one lead of said second substrate, and establishing electrical communication therebetween; and

encapsulating said first substrate and said second substrate with an encapsulation material.

2. (Currently amended) The method of claim 1, wherein ~~the step of~~ said attaching said first substrate to said second substrate further comprises ~~the steps of~~:

forming a passivation layer by said providing a passivation layer on said facing surface of said first substrate; and

attaching said passivation layer to said facing surface of said second substrate with a layer of adhesive.

3. (Currently amended) The method of claim 1, wherein ~~the step of~~ said attaching said first substrate to said second substrate further comprises:

forming a passivation layer by said providing a passivation layer on said facing surface of said second substrate; and

attaching said passivation layer to said facing surface of said first substrate with a layer of adhesive.

4. (Currently amended) The method of claim 1, wherein ~~the step of~~ said attaching said first substrate to said second substrate further comprises:

covering one of said first substrate and said second substrate with a glob top which adheres to the facing surface of one of said first substrate and said second substrate.

5. (Previously cancelled)

6. (Original) The method of claim 1, wherein at least one of said facing surface of said first substrate and said facing surface of said second substrate includes at least one groove thereon.

7. (Currently amended) The method of claim 1, wherein at least one of said first substrate and said second substrate comprises a ~~flip chip~~ flip-chip.

8. (Original) The method of claim 1, wherein at least one of said first substrate and said second substrate comprises a silicon wafer.

9. (Currently amended) An assembly method for a semiconductor assembly, comprising:

providing a first substrate having a first surface and having at least one lead having a portion thereof located on said first surface of said first substrate, said at least one lead having at least one conductive pad disposed on said portion thereof located on said first surface of said first substrate, said at least one conductive pad of said at least one lead of said first substrate having a substantially flat surface area and having a thickness;

providing a second silicon substrate having a first surface and having at least one lead having a portion thereof located on said first surface of said second silicon substrate, said at least one lead having at least one conductive pad disposed on said portion thereof located on said first surface of said second silicon substrate, said at least one conductive pad of said at least one lead of said second silicon substrate having a substantially flat surface area and having a thickness;

providing a passivation layer on said first surface of said first substrate, said passivation layer having a thickness greater than said thickness of the at least one conductive pad of said at

least one lead of said first substrate, said at least one conductive pad of said at least one lead of said first substrate being recessed a distance within said passivation layer;

forming an opening in said passivation layer at the location of said at least one conductive pad of said at ~~lest~~ least one lead of said first substrate;

attaching said first substrate to said second silicon substrate, said at least one conductive pad of said at least one lead of said second silicon substrate extending a distance within said opening in said passivation layer of said first substrate; and

abutting said substantially flat surface area of said at least one conductive pad of said at least one lead of said first substrate against said substantially flat surface area of said at least one conductive pad of said at least one lead of said second silicon substrate; and

forming a direct sliding movable contact between said substantially flat surface area of said at least one conductive pad of said at least one lead of said first substrate and said substantially flat surface area of said at least one conductive pad of said at least one lead of said second silicon substrate, and establishing electrical communication therebetween.

10. (Currently amended) The method of claim 9, wherein ~~the step of~~ said attaching said first substrate to said second silicon substrate further comprises:

forming a passivation layer by providing said passivation layer on said first surface of said first substrate; and

attaching said passivation layer to said first surface of said second silicon substrate with a layer of adhesive.

11. (Currently amended) The method of claim 9, wherein ~~the step of~~ said attaching said first substrate to said second silicon substrate further comprises:

forming a passivation layer by providing said passivation layer on said first surface of said second silicon substrate; and

attaching said passivation layer to said first surface of said first substrate with a layer of adhesive.

12. (Currently amended) The method of claim 9, wherein ~~the step of~~ said attaching said first substrate to said second silicon substrate further comprises:

covering a portion of one of said first substrate and said second silicon substrate with glob top material which adheres to the first surface of one of said first substrate and said second silicon substrate.

13. (Currently amended) The method of claim 9, wherein ~~the step of~~ said attaching said first substrate to said second silicon substrate further comprises:

encapsulating said first substrate and said second silicon substrate with an encapsulation material.

14. (Currently amended) The method of claim 9, wherein at least one of said first substrate first surface and said second silicon substrate first surface includes at least one groove thereon.

15. (Currently amended) The method of claim 9, wherein at least one of said first substrate and said second silicon substrate comprises a ~~flip chip~~ flip-chip.

16. (Currently amended) The method of claim 9, wherein at least one of said first substrate and said second silicon substrate comprises a silicon wafer.

17. (Currently amended) An assembly method for a semiconductor assembly, comprising:

providing a first silicon substrate having a plurality of leads on a first surface thereof, each lead of said plurality of leads of said first silicon substrate having a conductive pad disposed thereon in substantially a horizontal plane, each conductive pad of said first silicon substrate having a substantially flat surface area and having a thickness;

providing a second substrate having a plurality of leads on a first surface thereof in a substantially horizontal plane, each lead of said plurality of leads of said second substrate having a conductive pad disposed thereon, each conductive pad of said second substrate having a substantially flat surface area and having a thickness;

providing a passivation layer on said first surface of said first silicon substrate, said passivation layer having a thickness greater than said thickness of each conductive pad of said first silicon substrate, each said conductive pad of said first silicon substrate being recessed a distance within said passivation layer;

forming an opening in said passivation layer at ~~the~~ each location of said each conductive pad of said first silicon substrate;

attaching said first silicon substrate to said second substrate, each said conductive pad of said second substrate extending a distance within said opening in said passivation layer of said first silicon substrate; and

abutting said substantially flat surface area of said each conductive pad of said first silicon substrate against said substantially flat surface area of one said conductive pad of said second substrate; and

forming a direct sliding movable contact between said substantially flat surface area of said each conductive pad of said first silicon substrate and said substantially flat surface area of one said conductive pad of said second substrate, and establishing electrical communication therebetween.

18. (Currently amended) The method of claim 17, wherein ~~the step of~~ said attaching said first silicon substrate to said second substrate further comprises:

forming a passivation layer by said providing a passivation layer on said first surface of said first silicon substrate; and

attaching said passivation layer to said first surface of said second substrate with an adhesive.

19. (Currently amended) The method of claim 17, wherein ~~the step of~~ said attaching said first silicon substrate to said second substrate further comprises:

forming a passivation layer by said providing a passivation layer on said first surface of said second substrate; and

attaching said passivation layer to said first surface of said first silicon substrate with an adhesive.

20. (Currently amended) The method of claim 17, wherein ~~the step of~~ said attaching said first silicon substrate to said second substrate further comprises:

covering a portion of one of said first silicon substrate and said second substrate with glob top material which adheres to the first surface of one of said first silicon substrate and said second substrate.

21. (Currently amended) The method of claim 17, wherein ~~the step of~~ said attaching said first silicon substrate to said second substrate further comprises:

encapsulating said first silicon substrate and said second substrate with an encapsulation material.

22. (Currently amended) The method of claim 17, wherein at least one of said first silicon substrate first surface and said second substrate first surface includes at least one groove thereon.

23. (Currently amended) The method of claim 17, wherein at least one of said first silicon substrate and said second substrate comprises a ~~flip chip~~ flip-chip.

24. (Currently amended) The method of claim 17, wherein at least one of said first silicon substrate and said second substrate comprises a silicon wafer.

25. (Currently amended) An assembly method for a semiconductor assembly, comprising:

providing a first silicon wafer substrate having a plurality of leads on a first surface thereof, each lead of said plurality of leads of said first silicon wafer substrate having a conductive pad disposed on a portion thereof in substantially a horizontal plane, each conductive pad of said first silicon wafer substrate having a substantially flat surface area and having a thickness;

providing a second silicon wafer substrate having a plurality of leads on a first surface thereof in a substantially horizontal plane, each lead of said plurality of leads of said second silicon wafer substrate having a conductive pad disposed thereon, each conductive pad of said second silicon wafer substrate having a substantially flat surface area and having a thickness;

providing a passivation layer on said first surface of said first silicon wafer substrate, said passivation layer having a thickness greater than said thickness of each said conductive pad of said first silicon wafer substrate, each said conductive pad of said first silicon wafer substrate being recessed a distance within said passivation layer;

forming an opening in said passivation layer for said each conductive pad of said first silicon wafer substrate;

attaching said first silicon wafer substrate to said second silicon wafer substrate, each said conductive pad of said second silicon wafer substrate extending a distance within said opening in said passivation layer of said first silicon wafer substrate; ~~and~~

abutting said substantially flat surface area of said each conductive pad of said first silicon wafer substrate against said substantially flat surface area of one said conductive pad of said second silicon wafer substrate; and

forming a direct sliding movable contact between said substantially flat surface area of said each conductive pad of said first silicon wafer substrate against said substantially flat surface area of one said conductive pad of said second silicon wafer substrate, and establishing electrical communication ~~therebetween .~~ therebetween.

26. (Currently amended) The method of claim 25, wherein ~~the step of~~ said attaching said first silicon wafer substrate to said second silicon wafer substrate further comprises:

forming a passivation layer by providing said passivation layer on said first surface of said first silicon wafer substrate; and

attaching said passivation layer to said first surface of said second silicon wafer substrate with an adhesive.

27. (Currently amended) The method of claim 25, wherein ~~the step of~~ said attaching said first silicon wafer substrate to said second silicon wafer substrate further comprises:

forming a passivation layer by providing said passivation layer on said first surface of said second silicon wafer substrate; and

attaching said passivation layer to said first surface of said first silicon wafer substrate with an adhesive.

28. (Currently amended) The method of claim 25, wherein ~~the step of~~ said attaching said first silicon wafer substrate to said second silicon wafer substrate further comprises:

covering a portion of one of said first silicon wafer substrate and said second silicon wafer substrate with glob top material which adheres to the first surface of one of said first silicon wafer substrate and said second silicon wafer substrate.

29. (Currently amended) The method of claim 25, wherein ~~the step of~~ said attaching said first silicon wafer substrate to said second silicon wafer substrate further comprises:

encapsulating said first silicon wafer substrate and said second silicon wafer substrate with an encapsulation material.

30. (Currently amended) The method of claim 25, wherein at least one of said first silicon wafer substrate first surface and said second silicon wafer substrate first surface includes at least one groove thereon.

31. (Currently amended) The method of claim 25, wherein at least one of said first silicon wafer substrate and said second silicon wafer substrate comprises a ~~flip-chip~~ flip-chip.

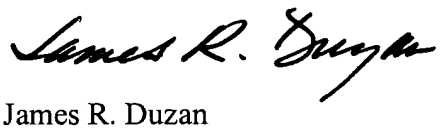
32. (Previously cancelled)

REMARKS

This amendment corrects errors in the text. Entry is respectfully solicited.

This amendment is submitted prior to or concurrently with the payment of the issue fee and, therefore, no petition or fee is required. No new matter has been added.

Respectfully submitted,



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